

8040

40Gbit/s SONET/SDH ADM-on-a-Chip with Integrated Cross-Connect

Product Brief :

The Network is the Experience™

The 8040 is a SONET/SDH ADM-on-a-chip CMOS IC characterized by high integration and low power that operates as an OC-192/STM-64 SONET/SDH add-drop multiplexer (ADM). The 8040 is designed as a system-on-a-chip integration of all the functionality of a conventional SONET ADM system, onto a single piece of silicon. The device has a total of 10 ports, with 2 high-speed line interfaces running at OC-192/STM-64 and 8 low-speed add/drop ports that are software configurable to run at OC-3/STM-1, OC-12/STM-4 or OC-48/STM-16.

All 10 port interfaces provide complete read/write access to section and line overhead, path trace access, pointer processing, alarm detection and insertion, and section, line, and path performance monitoring (PM). A full 40Gb/s STS-1/STM-0 cross-connect is provided across all interfaces. The physical interfaces are based on LVDS technology, with a variety of programmable bus width and speed combinations. In addition to fully compliant traditional SONET functionality, extra built-in features enable next generation SONET features such as virtual rings, multi-ring termination and SONET mesh. The combination of standards support and new generation features allows systems to be deployed in a legacy environment and then upgraded to enable next generation features with only a software change.

FEATURES

Overview

- ADM-on-a-chip incorporating dual line side interfaces and eight tributary interfaces with integrated STS-1/STM-0 granular cross-connect
- Applications range from next generation SONET/SDH ADM/DCS elements to integrated ADM-on-a-blade for existing DWDM systems
- Support for multi-chip configurations for larger port count systems
- Configurable low-speed mode for OC-48/STM-16 ADM functionality

Line & Tributary Ports

- 8 low-speed (tributary) ports, independently software programmable to OC-3/12/48 (STM-1/4/16)
- Two 10Gb/s high speed (line) ports, OC-192 (STM-64)
- Handles all concatenation levels of STS Mc, ($2 < M < 192$), e.g., 2c, 7c, 24c, and any valid mix of STS-1 and concatenated payloads, making it ideal for data over SONET applications
- Section/line termination/generation of all traffic on all 10 ports, with pointer processing and frame alignment on all ports
- Ability to force path AIS and UNEQ on any STS-1 under software control

Cross-Connect

- Full STS-1/STM-0 granular transport-level processing and non-blocking cross-connect (40G x 40G) with hitless grooming across all ports and all time slots (full TSI)
- On-chip connection memory for flexible, hitless configuration of working and protection configurations for each STS-1/STM-0
- Support for hairpinning, broadcast, multi-cast, drop-and-continue and full TSI

Overhead Access

- Support for automatic protection switching:
 - K1/K2 byte access and BER monitoring
 - Support for 1+1, 1:1, 1:N, UPSR, and BLSR protection mechanisms
 - Flexible protection schemes
- Flexible Transport overhead byte extraction/insertion with dedicated interface to external overhead processor, on all ports. Provides for easy adaptation to changes in standards, as well as interoperability with existing proprietary equipment, with no hardware changes.
- On-chip electric wavelength (overlay ring) support, including TOH byte forwarding and error condition preservation
- SONET/SDH compliant performance monitoring, condition and alarm reporting
- Optional insertion and extraction of additional "undefined" overhead bytes as a private communication channel (PCC) with dedicated interface to external communications processor. PCC is a superset of the ELDC standard.
- Path Monitoring on all incoming traffic per GR-1400-CORE (B3, C2, J1), with STS-1 granularity for paths



Interfaces

- 622 MHz LVDS I/O - OIF SFI-4 compatible interfaces for high speed ports, enabling direct connection to SERDES
- Flex programmable LVDS bus technology, with programmable I/O bus width and speeds, including support for OIF SFI-4
- Full set of diagnostic loopbacks on all ports

Physical

- 16-bit general-purpose host/system interface for configuration, control and status monitoring
- Built-in loopbacks at multiple points
- IEEE 1149.1 port with scan and JTAG boundary scan
- Low power CMOS 1.2V core with 2.5/3.3V I/O
- 1405 pin, 39x39mm flip-chip BGA package
- Power dissipation: 8W max , 6.4W typical

Diagnostics and Fault Isolation Support

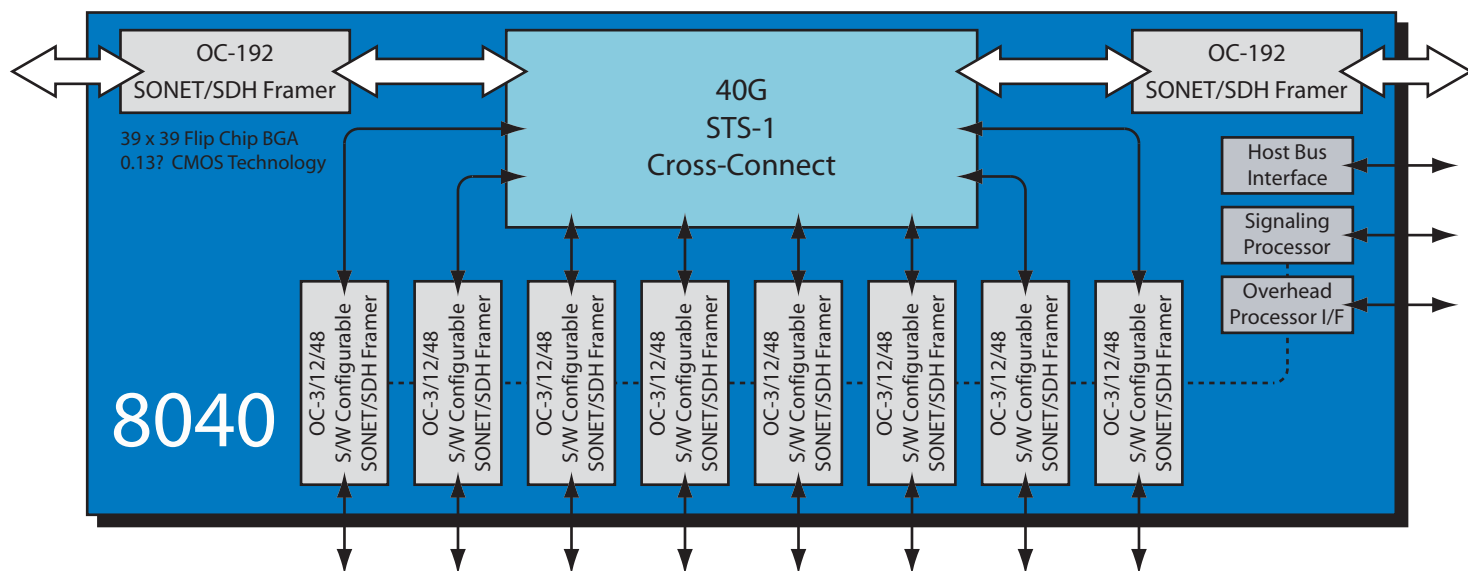
- Loopback capabilities
- Ability to insert parity errors
- Ability to insert framing errors
- Ability to detect loss of clock failure (no toggling) on LVDS clock inputs and 8KHz frame sync input
- Indicate PLL lock state (and loss of main clock) via external pin, since error reporting, interrupts, and/or software access to registers is disrupted by loss of the main clock
- Parity generation and checking on all external interfaces
- Full audit capability: ability to read back both the active and inactive banks of configuration registers and tables

Standards Compliance (Telcordia, ANSI, and ITU)

- GR-253-CORE, SONET Transport Systems: Common Generic Criteria
- GR-496-CORE, SONET Add-Drop Multiplexer (SONET ADM) Generic Criteria
- GR-1230-CORE, BLSR
- GR-1400-CORE, UPSR
- ITU-T G.707: Network Node Interface for the Synchronous Digital Hierarchy
- ITU-T G.803: Architecture of Transport Networks Based on the Synchronous Digital Hierarchy
- ANSI T1.105

Applications

- Next generation SONET/SDH terminal equipment (ADM)
- Metro digital cross connect systems
- SONET aggregation multiplexers
- GbE transport multiplexers
- ADM-on-a-Blade for DWDM systems
- Stand-alone element in a single stage switching system (a.k.a. "pizza box")



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Some features listed in the specifications are under development.

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